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Research Article

Top gate engineering of field-effect transistors based on wafer-scale two-dimensional semiconductors

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ABSTRACT

The investigation of two-dimensional (2D) materials has advanced into practical device applications, such as cascaded logic stages. However, incompatible electrical properties and inappropriate logic levels remain enormous challenges. In this work, a doping-free strategy is investigated by top gated (TG) MoS_2 field-effect transistors (FETs) using various metal gates (Au, Cu, Ag, and Al). These metals with different work functions provide a convenient tuning knob for controlling threshold voltage (V_{th}) for MoS_2 FETs. For instance, the Al electrode can create an extra electron doping (n-doping) behavior in the MoS_2 TG-FETs due to a dipole effect at the gate-dielectric interface. In this work, by achieving matched electrical properties for the load transistor and the driver transistor in an inverter circuit, we successfully demonstrate wafer-scale MoS_2 inverter arrays with an optimized inverter switching threshold voltage (V_M) of 1.5 V and a DC voltage gain of 27 at a supply voltage (V_{DD}) of 3 V. This work offers a novel scheme for the fabrication of fully integrated multistage logic circuits based on wafer-scale MoS_2 film.

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1. Introduction

Incumbent technologies beyond Si complementary metal-oxide-semiconductor (CMOS), including amorphous Si [1], carbon nanotube [2], and metal oxides [3,4], have been vastly developed during the past decades. Since graphene was discovered in 2004 [5], its extraordinary properties have inspired extensive research into next-generation transistors and integrated circuits (ICs) [6]. Although graphene possesses the highest intrinsic carrier mobility among the two-dimensional (2D) material family [7], its small on/off current ratio on account of the gapless band structure makes it inappropriate for fabricating digital ICs that require ideal Boolean “0” and “1” states at room temperature [8,9]. MoS_2, on the other hand, is a typical semiconductive transition-metal dichalcogenide (TMD) with a suitable bandgap in the range of 1.2 to 1.8 eV depending on its thickness [10,11]. The isolation of a MoS_2 monolayer via mechanical exfoliation [12–14] allows early demonstration of field-effect transistors (FETs) with a superior current on/off ratio that can exceed 10^8, making it promising for logic devices [15–19] and low-power electronics applications [20]. Its 2D nature also enables dimensional scaling down following Moore’s law [21]. Recently, research on 2D semiconductors has begun to translate from the fundamental investigation into rudimentary functional circuits. Thus wafer-scale material synthesis and practical device processing become more critical. Recently monolithic integrated circuits with simple logic functions have been demonstrated based on mechanically exfoliated micro-scale MoS_2 sheets [22–24] or MoS_2 film synthesized by chemical vapor deposition (CVD) [19,25,26]. Nevertheless, it is still difficult to precisely control the threshold voltage (V_{th}) of MoS_2 FETs to achieve appropriate logic levels satisfying the requirement of cascaded logic stages, which are crucial for large-scale digital ICs [27,28]. For instance, one basic logic element is an inverter gate, and the primary method for the inverter design is by tuning the driver-to-load ratio of the two transistors. Therefore, the manipulation of V_{th} for the MoS_2 FET is essential, and its technology can be extended to other 2D semiconductors for future circuit-level processing and design of 2D electronics [29].

Ion implantation is a conventional CMOS processing method for bulk Si, but it is unsuitable for 2D semiconductors since it brings severe lattice damage to their crystal lattices [30]. Various methods have been developed for modifying the doping level of 2D-TMD to tune V_{th}. One method is to adjust the width to length ratio (W/L) [31], which is commonly used to improve overall transistor match-

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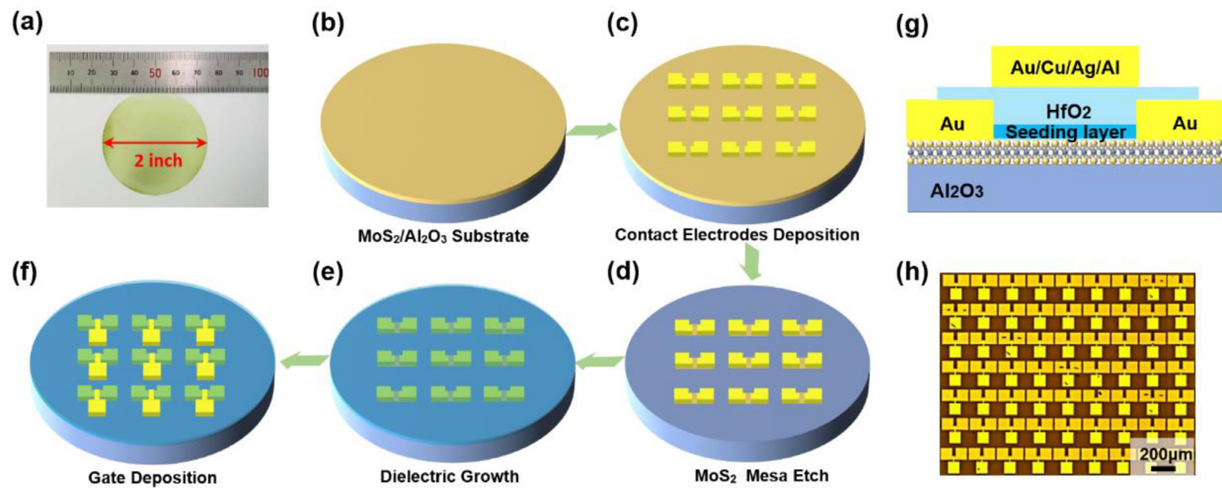

Fig. 1. Fabrication process and schematic illustration of the device structure. (a) Photograph of a two-inch sapphire wafer uniformly covered by monolayer MoS_2 film grown by CVD. (b-f) A brief fabrication process of MoS_2 to gated FETs employing metal gates with different work functions. (g) Schematic cross-section of the MoS_2-based FET. (h) Optical microscopy image of the MoS_2 TG-FET array on a diced 1 cm × 1 cm wafer. The scale bar is 200 μm.

ing in terms of V_{th} [32]. However, the limitation is that V_{th} can only be effectively modified within a limited range, and the expected suitable ratio is difficult to obtain because it will further increase the area occupied by the combinational logic gates. Therefore, if V_{th} can be adjusted via a simple processing method rather than changing the dimensions of the transistors, the circuit design will be much more convenient.

By choosing different materials for the dielectric layer on top of the 2D-TMD channel, V_{th} can also be modified by the interface charge impurities or dipoles in the dielectric layer [27,33]. However, the complex dielectric stack structure normally suffers from poor stability [34]. In Si CMOS processing, it is generally acknowledged that metal gates with different work functions can control the V_{th} of FETs [35], and have also been studied in exfoliated 2D-TMD devices [36]. For instance, Al and Pt gates have been used to modulate the V_{th} of MoS_2 FETs in the negative and positive directions, respectively [15]. Nevertheless, there has been no systematic investigation into the effect of metal gates with different work functions on wafer-scale continuous 2D semiconductors and their logic devices.

In this work, an optimized device configuration is proposed to design logic gates on wafer-scale 2D-MoS_2 by engineering the work functions of top gate (TG) metals. Through methodically investigating the influence of metal gates composed of different metals (Au, Cu, Ag, and Al) on the performance of MoS_2 FETs, a robust and consistent V_{th} deviation is observed, and the dipole effect induced by an Al gate is further investigated. With the capabilities of fulfilling a suitable V_{th} and a reliable logic level, the MoS_2-based inverter is demonstrated with an optimized switching threshold voltage (V_M) of 1.5 V and the highest voltage gain of 27 at a supply voltage (V_{DD}) of 3 V. This demonstration of logic devices provides a platform for large-scale cascaded logic stages based on MoS_2 and other 2D semiconductors, offering a bright future for complex logic applications.

2. Materials and methods

To demonstrate that our method can be utilized to fabricate large-scale MoS_2-based digital ICs, we fabricate our devices on a large-scale monolayer MoS_2 film grown by CVD on a two-inch sapphire wafer, as shown in Fig. 1(a), which has been confirmed to possess excellent material properties [19]. Atomic force microscopy (AFM) imaging and Raman spectra under the irradiation of a 514 nm laser are shown in Fig. S1. The thickness of the as-grown MoS_2 film is approximately 0.75 nm, which is consistent with the typical thickness of a MoS_2 monolayer, and the difference between E^1_{2g} and A_{1g} peaks is 20 cm^{-1} [37]. A brief device fabrication process is illustrated in Fig. 1(b-f). For the convenience of processing, the two-inch wafer is sliced into 1 cm × 1 cm pieces. The source and drain electrodes are firstly formed by deposition of the 35-nm Au layer, and the MoS_2 channel is then etched to the designated dimensions (W/L = 30 μm/20 μm). The subsequent step is to deposit the seeding layer (SL), which has been investigated as an interface engineering method and can assist to form a uniform high-k layer [38], followed by the growth of the HfO_2 gate dielectric layer with a thickness of 16 nm. The Au metal with the work function of 5.1 eV, as well as Cu (4.65 eV), Ag (4.3 eV), and Al (4.08 eV), are deposited as gate metals. The optical microscopy image of the MoS_2 FET array fabricated on the sapphire substrate is shown in Fig. 1(h), in which all the FETs are designed to share the same geometric size.

3. Results and discussion

3.1. Electrical performance of MoS_2 TG-FETs with different metal gates

TG metals with different work functions have been examined to modulate the electrical characteristics of Si FETs [35,39], and this approach is also feasible to be applied in MoS_2 FETs. All the MoS_2 FETs exhibit typical n-type transistor behavior at room temperature, and typical transfer characteristics (I_D-V_{TG}) of MoS_2-based FETs with four different types of metal gates are plotted in Fig. 2(a) (see Fig. S2 for more details). It is noteworthy that our TG device processing provides a satisfactory level of device homogeneity for each type of TG metal. All the devices exhibit efficient gate modulation with the current on/off ratio reaching approximately 10^8, which is important for reducing the static power consumption in logic devices. For on-state driving current (I_{on}), it is also noticeable that I_{on} increases with the reduction in the work function of the metal gate as V_{th} decreases, which is consistent with previous studies [35].

The statistical results of the V_{th} distribution for different metal gates are illustrated in Fig. 2(b) (V_D = 0.2 V). Here, the V_{th} value is determined by $V_{th}=V_{GS}-\frac{I_D}{g_{max}}-\frac{V_D}{2}$ based on the transfer curve [19]. The MoS_2 FETs with Al gates exhibit an average V_{th} of 0.9 V, and the average V_{th} of the transistors with Ag, Cu, and Au gates are

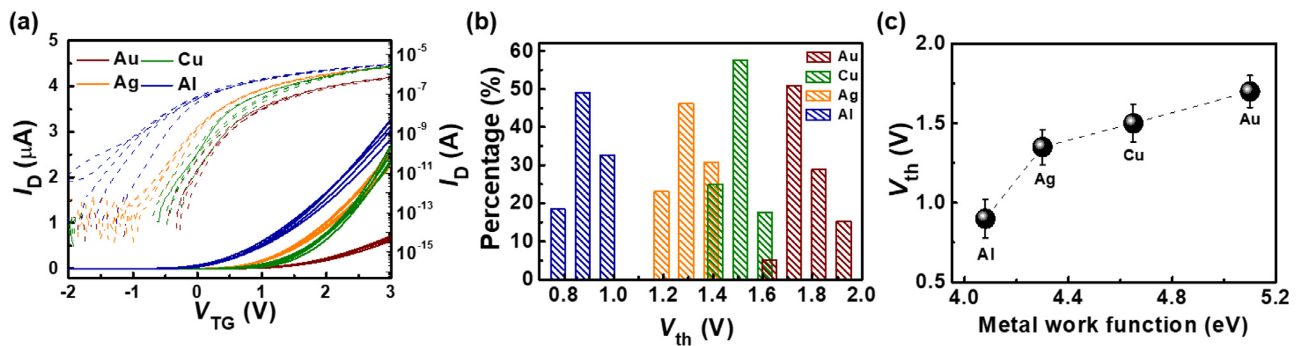

Fig. 2. Transfer characteristics of MoS_2 FETs with different metal TG electrodes. (a) Transfer curves ($V_D = 0.2$ V) of the transistors in linear scale (left *Y*-axis) and logarithmic scale (right *Y*-axis) with Au (5.1 eV), Cu (4.65 eV), Ag (4.3 eV), and Al (4.08 eV) gates, respectively. (b) Statistical result of the V_{th} of MoS_2 FETs with four different metal gates (30 random samples for each type of metal). (c) Average V_{th} versus metal gate work function.

1.35, 1.5, and 1.7 V, respectively. A plot of the average V_{th} versus metal gate work function is illustrated in Fig. 2(c), in which the average V_{th} has a monotonic relationship with the work function values for Ag, Cu, and Au. It is also noteworthy that for FETs fabricated with Al gate, the average value of V_{th} has an evident decrease, which is possibly attributed to the increase in the amount of positive charge induced in the dielectric layer due to the oxidation of the Al electrode at the Al/HfO_2 interface, which will be further discussed below.

3.2. Dipole effect in the gate dielectric layer

For FETs with a metal/high-*k*/SL stack TG structure, several origins for V_{th} deviation have already been discussed, including the influence of top interface dipoles at the gate/high-*k* interface, dipoles due to the oxygen vacancy (Vo) in the high-*k* dielectrics, and the bottom interface dipoles at the high-*k*/SL interface [28]. This section focuses on investigating the correlation of V_{th} shift with dipoles induced by Vo in the HfO_2 gate dielectric layer.

To investigate the existence of the Vo more straightforward, the TG region of the MoS_2 transistor with an Al gate is characterized by the high-resolution transmission electron microscope (HRTEM) and high-angle annular dark-field (HAADF) scanning transmission electron microscope (STEM). As shown in the cross-sectional image (Fig. 3(a)) and the zoom-in of a small portion of the Al/HfO_2 interface (Fig. 3(b)), a thin Al_2O_3 interlayer is present between the Al TG electrode and the HfO_2 gate dielectric layer. In addition, the energy-dispersive X-ray spectroscopy (EDS) element mapping distinctly presents the chemical composition, including the Al TG electrode, Al_2O_3 interlayer, and HfO_2 dielectric layer, as shown in Fig. 3(c). It is clearly shown that the thin Al layer at the Al/HfO_2 interface is oxidized to a dense Al_2O_3 layer by taking the oxygen atoms from HfO_2, resulting in generating more Vo in the HfO_2 dielectric layer. Moreover, because of the dense structure, Al_2O_3 can act as a passivation layer, so the thickness of the Al_2O_3 layer will not become thicker after reaching a maximum of about 4 nm, and a stable thickness can be maintained. It is also noteworthy that the results from previous studies have confirmed that the bottom high-*k* HfO_2 layer determines the shift of V_{th} for an Al_2O_3/HfO_2 stack [28]. Compared to the original HfO_2 layer with only a few positive charges [40,41], the Vo generated in the HfO_2 layer leads to additional surplus positive charges, and hence the dipoles are induced by this relevant charge transfer as illustrated in Fig. 3(d). This is possibly the main reason of the significant V_{th} shift in the negative direction for n-type MoS_2-based FETs.

Furthermore, different metal gates are used to control the V_{th} of the MoS_2-based FETs, and three typical band diagrams are illustrated in Fig 3(e). Without any gate bias, the metal gate that possesses a lower work function than the MoS_2 semiconductor tends to induce electron accumulation in the channel. However, the metal gate with a higher work function results in a charge depletion state for the channel. The shift in the V_{th} of those MoS_2 transistors with Ag and Au gates is approximately 0.35 V. In addition, the induced dipole influence in Al gates can also be analyzed in a band diagram, considering the mechanism mentioned above. More specifically, more positive charges in the HfO_2 gate dielectric layer can introduce more electrons to accumulate in the channel and further cause the energy band of the MoS_2 interface to bend down. An optimized n-doping behavior in the MoS_2 channel and an effective reduction in the corresponding V_{th} are then observed.

3.3. Electrical characterization of MoS_2-based logic inverter

Most MoS_2 FETs exhibit an n-type behavior because it is dominated by sulfur vacancies that result in the intrinsic electron concentration [42]. We then fabricate MoS_2-based logic inverters which consist of one n-type load (pull-up) and one n-type driver (pull-down) transistor. The two MoS_2 FETs are designed with the same aspect ratio ($W/L = 30$ μm/20 μm) but different metal gates, thus enabling different V_{th} in the load and driver transistors. The cross-sectional configuration of the inverter device is illustrated in Fig. 4(a). The load transistor with Al TG has an optimized V_{th} as mentioned in the previous section and acts as a nonlinear resistor. The driver transistor with Au TG performs the function of a voltage switch. Fig. 4(b) shows the optical microscopic image and circuit diagram of the inverter, whose fabrication procedure is similar to the one illustrated in Fig. 1, except for one additional step of etching a via-hole to connect the gate of the load transistor directly to its source electrode. More details on the inverter fabrication process are provided in the Supplementary Materials.

The stable transfer characteristics of the MoS_2 FETs with Al and Au gates are shown in Fig. 4(c), and there is a 0.75 V shift of V_{th} between them due to the dipole effect induced by the Al TG. Although the calculated V_{th} of the MoS_2 FETs with Al TG is a positive V_{th} of about 0.8 V, showing the enhancement mode, it has a significantly larger current in the sub-threshold region than the device with Au TG. Upon sweeping V_{TG} from -3 to $+3$ V, both transistors have a high on/off current ratio above 10^8, and the subthreshold swing (SS) is about 160 mV dec^{-1}. Such efficient electrostatic control at room temperature contributes to the large voltage gain of the inverter, which is crucial to its anticipated logic switching performance because it enables the inverter to drive the cascaded logic gates without a signal restoration. The output characteristics of both transistors are shown in Fig. 4(d), which indicates that the drain current (I_D) of both transistors tends to saturate at high electric fields. Moreover, the on-state current of the load transistor with an Al gate is though as small as about 150 nA, but is much higher than that with an Au gate at zero gate bias, which is ben-

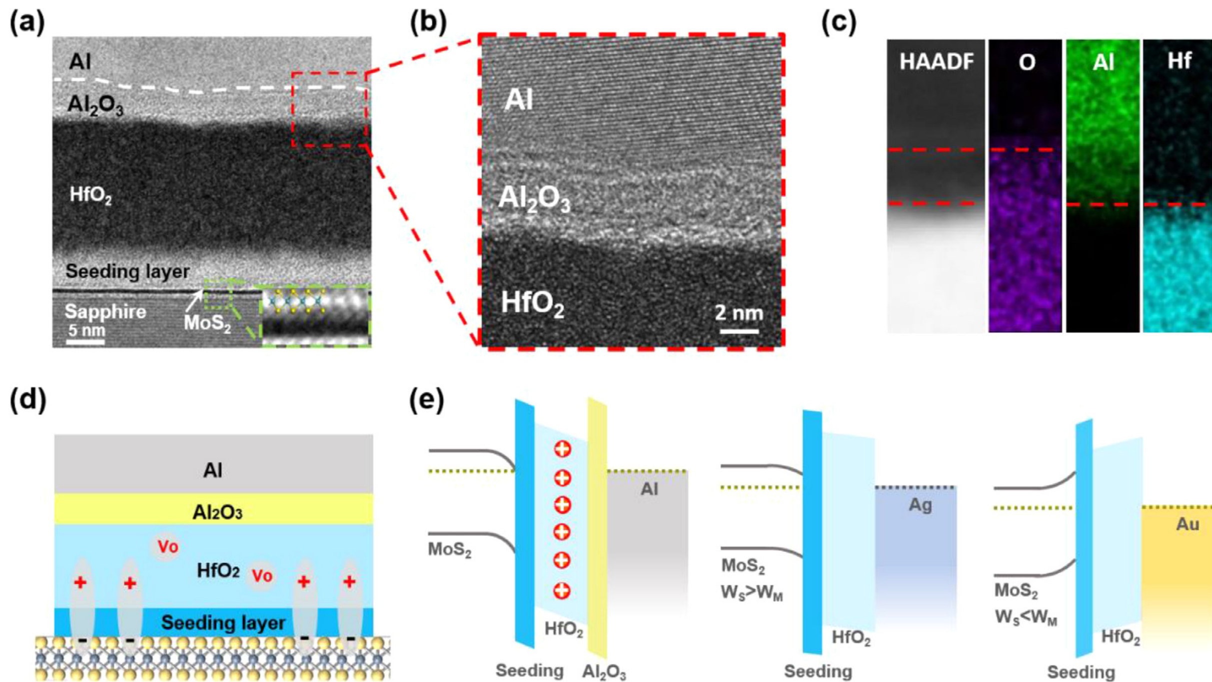

Fig. 3. Characterization of the dipole effect induced in MoS_2-based FETs with Al gates. (a) Cross-sectional HRTEM image of the Al gate region. (b) Zoom-in of the Al/HfO_2 interface, which confirms the oxidation of the Al gate at the interface. (c) Cross-sectional HAADF image and the corresponding EDS element mappings of the Al/HfO_2 interface. (d) Schematic illustration of the dipole due to Vo for the Al_2O_3/HfO_2/SL/MoS_2 stack structure. (e) Vertical schematic flat-band diagrams of the MoS_2 transistors with Al, Ag, and Au gates at zero gate bias. For metal gates with different work functions, the channel is under either accumulation or depletion regions. Furthermore, the band diagram of those with Al gates indicates the dipole effect occurring in the gate dielectric layer.

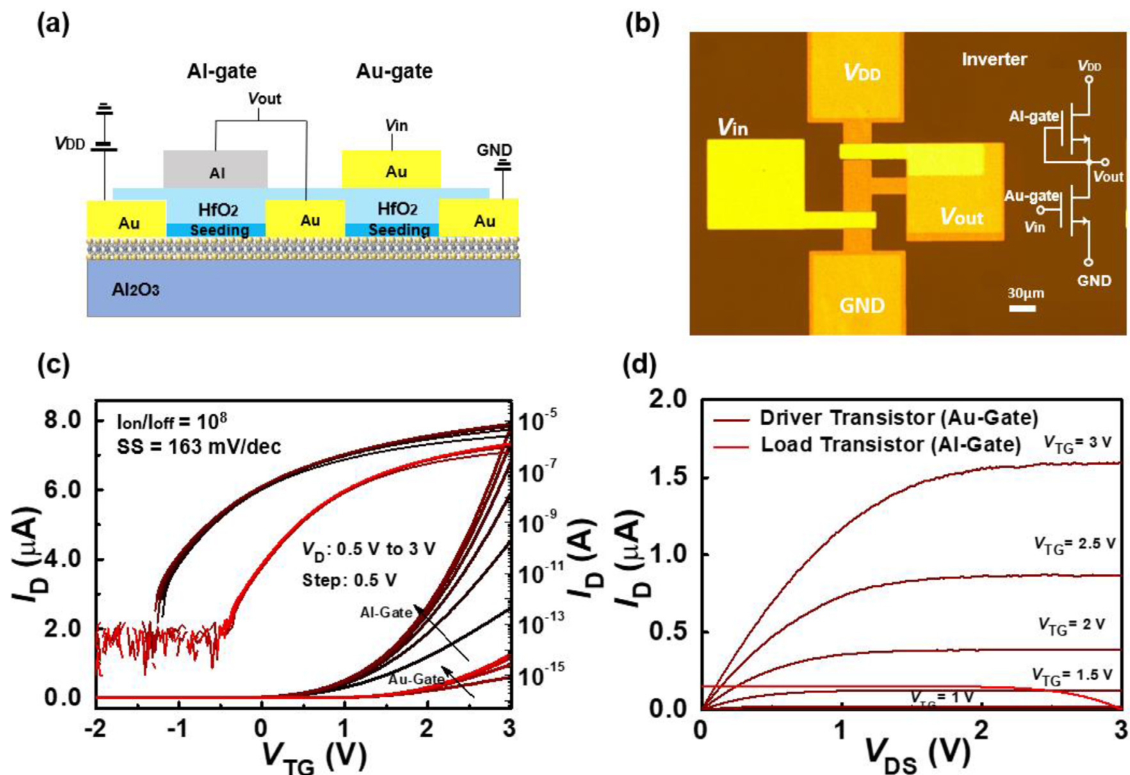

Fig. 4. Electrical characterization of the MoS_2-based inverter. (a) Schematic diagram of the inverter circuit configuration in cross-section and the corresponding electrical measurement setup. (b) Optical microscopy image of the inverter. Scale bar is 30 μm. (c) Transfer curves of the load and driver MoS_2-based FETs in linear scale (left *Y*-axis) and logarithmic scale (right *Y*-axis). The load transistor has an Al gate, whereas the driver transistor has an Au gate. The difference between the work function of Al and Au results in a 0.75 V shift in V_{th}. (d) Output characteristics of the driver transistor with Au gate (the purple curves) and the load characteristic of the load transistor with Al gate (the red curve).

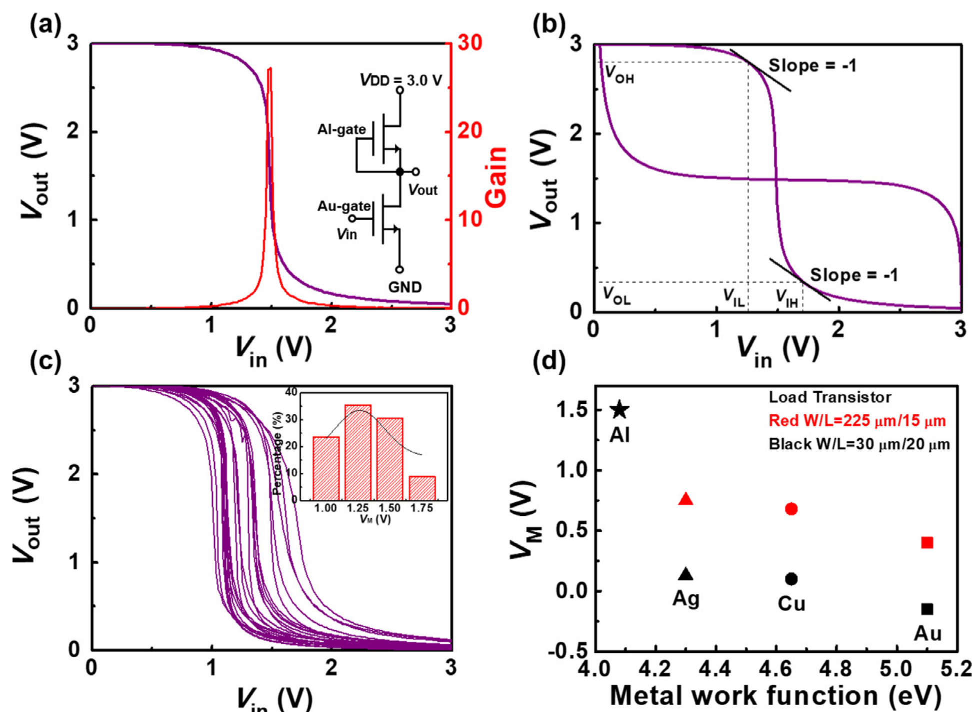

Fig. 5. Characteristics of the MoS_2-based inverter. (a) Voltage transfer characteristic of the inverter (purple curve) and the corresponding voltage gain (red curve). Inset is the circuit diagram of the inverter. (b) Bi-stable hysteresis voltage transfer characteristics of the inverter. V_{OH} represents the minimum high output voltage when the output level is logic "1"; V_{OL} represents the maximum low output voltage when the output level is logic "0"; V_{IL} represents the maximum low input voltage, which can be interpreted as logic "0"; and V_{IH} represents the minimum high input voltage, which can be interpreted as logic "1". (c) The distribution of the voltage transfer characteristics of the inverter. Inset shows the histogram of the V_M shift and the Gaussian fit for 30 MoS_2-based inverters based on the statistical database. (d) Relationship between average V_M and work function of the load transistor metal gates (Au, Cu, Ag, and Al). The MoS_2-based inverters composed of load transistor with W/L = 30 μm/20 μm (black dots) and W/L = 225 μm/15 μm (red dots) are further compared. All the driver transistors have the same Au gate and the identical W/L of 30 μm/20 μm.

eficial to obtain a good static response of the inverter, such as V_M and the noise margin.

In principle, the performance of the MoS_2-based inverter circuit can be predicted by the isolated load and driver transistors, which have been examined in the previous section to exhibit matched V_{th} and I_D saturation. The voltage transfer characteristic of the inverter and the corresponding voltage gain as a function of input voltage are shown in Fig. 5(a) (V_{DD} = 3 V), which indicates an appropriate V_M of 1.5 V and a maximum voltage gain of 27. To characterize the robustness of the inverter, the noise margin for low input signal levels (NM_L) and high input signal levels (NM_H) are extracted as illustrated in Fig. 5(b). When the V_{DD} of the inverter is 3 V, it can be observed that the corresponding NM_L is 0.91 V and NM_H is 1.1 V, indicating that the inverter has a much higher tolerance to noise [9,19]. Hence, the inverter designed here is reliable in more complex multistage logic gate circuits. Moreover, from the statistical analysis of voltage transfer curves (Fig. 5(c)), it is apparent that the distribution of V_M is relatively narrow. The V_M concentrates in the range of 1 V to 1.75 V, which indicates a reliable integration of Al gate and Au gate for the MoS_2-based inverter. Besides, the statistics of the V_M are shown in Fig. 5(c) in the form of a histogram by testing 30 random MoS_2-based inverter samples. The transition of our MoS_2-based inverter occurs when the input voltage (V_{in}) approaches half of the V_{DD}, which is virtually an ideal NOT logic gate with a high noise margin. Therefore, it is advantageous for multistage logic gates and more complex combinational logic circuits.

On the other hand, the W/L of the FET channel can also influence the V_M. As shown in Fig. S3, by sizing up the transistor with a W/L of 225 μm/15 μm, which is 10 times larger than the preceding transistor (W/L = 30 μm/20 μm), the V_{th} of the transistor with the same Au gate is observed to shift 0.5 V in the negative direction. Hence, the voltage transfer characteristics of the MoS_2-based inverter composed of load transistor with two different W/Ls (30 μm/20 μm and 225 μm/15 μm) and three different metal gate materials (Au, Cu, and Ag) are compared in Fig. S4. The statistics of the corresponding average V_M are plotted in Fig. 5(d), and the value of V_M is observed to increase with decreased metal gate work function and increased load transistor W/L. The regulation of the W/L can only shift the V_M in a limited range, and a large channel W/L significantly increases the circuit area. In comparison, tuning the work function of the metal gate is more efficient. Therefore, by utilizing the specific Al gate or other stable metal gates combined with the design of the channel W/L for the MoS_2-based inverter, it is feasible to implement cascaded logic gates based on the inverter with the desired performance.

4. Conclusion

In conclusion, this work not only systematically investigates the influence of metal gates with different work functions on the electrical performance of MoS_2-based FETs, but also validates the fundamental dipole effect induced in the gate dielectric layer caused by the oxidation of the Al TG electrode. Through the comprehensive analysis of the Al/HfO_2 interface and the corresponding band structure, the importance of the positively charged Vo in the gate dielectric layer to the electrical characteristics of MoS_2-based transistor is further demonstrated. In addition, with the optimized match of the V_{th} of the load transistor with an Al gate and the driver transistor with an Au gate, an inverter with an optimized V_M of 1.5 V and a maximum voltage gain of 27 is successfully achieved. Based on the mechanism of modulating the MoS_2-based inverter's V_M proposed in our research combined with increasingly mature CVD techniques for MoS_2 film growth, the monolithic integration

of more complex MoS_2-based cascaded logic gates is hopefully anticipated.

Author contributions

Wenzhong Bao and Chenjian Wu conceived and supervised the research. Jingyi Ma designed, fabricated, and tested the MoS_2 devices and wrote the manuscript. Xinyu Chen and Yaochen Sheng designed the experiments and analyzed the characterizations. Ling Tong, Xiaojiao Guo, and Minxing Zhang revised the manuscript. Chen Luo measured the TEM images. Lingyi Zong, Yin Xia, Chuming Sheng, Yin Wang, Saifei Gou, and Xinyu Wang participated in the discussion during the development of the paper. Peng Zhou, Xing Wu, and Wei David Zhang presented suggestions for improving the quality of this work. All authors examined and commented on the manuscript.

Declaration of Competing Interest

The authors declare that they have no conflict of interest.

Acknowledgments

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Supplementary materials

Supplementary material associated with this article can be found, in the online version, at doi:10.1016/j.jmst.2021.08.021.

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