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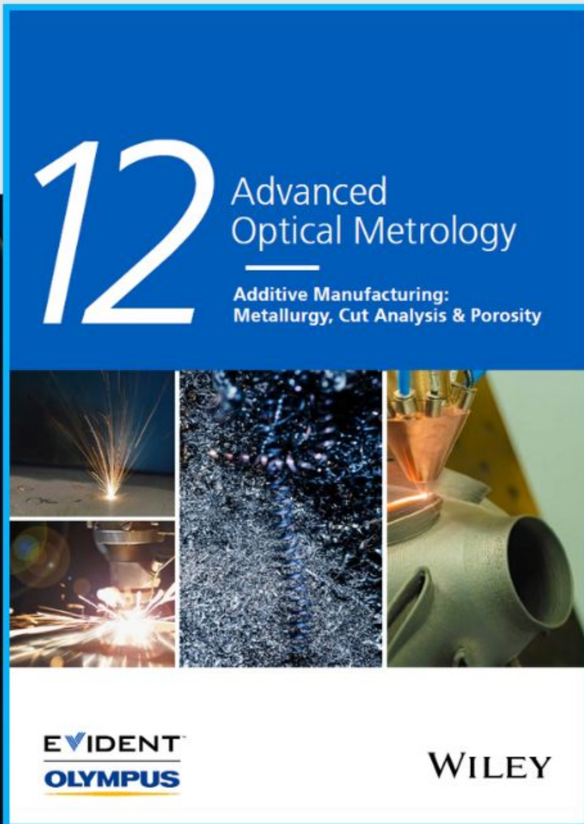

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Wafer-Scale Demonstration of MBC-FET and C-FET Arrays Based on Two-Dimensional Semiconductors

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Two-dimentional semiconductors have shown potential applications in multi-bridge channel field-effect transistors (MBC-FETs) and complementary field-effect transistors (C-FETs) due to their atomic thickness, stackability, and excellent electrical properties. However, the exploration of MBC-FET and C-FET based on large-scale 2D semiconductors is still lacking. Here, based on a reliable vertical stacking of wafer-scale 2D semiconductors, large-scale MBC-FETs and C-FETs using n-type MoS_2 and p-type $MoTe_2$ are successfully fabricated. The drive current of an MBC-FET with two layers of MoS_2 channel (20 µm/10 µm) is up to 60 µA under 1 V bias. Compared with the single-gate MoS_2 FET, the carrier mobility of MBC-FET is 2.3 times higher and the sub-threshold swing is 70% smaller. Furthermore, NAND and NOR logic circuits are also constructed based on two vertically stacked MoS_2 channels. Then, C-FET arrays are fabricated by 3D integrating n-type MoS_2 FET and p-type $MoTe_2$ FET, which exhibit a voltage gain of 7 V/V when V_{DD} = 4 V. In addition, this C-FET device can directly convert light signals to an electrical digital signal within a single device. The demonstration of MBC-FET and C-FET based on large-scale 2D semiconductors will promote the application of 2D semiconductors in next-generation circuits.

1. Introduction

The progress of Moore's Law along with the incessant prevalence and thriving development of electronic technology have provided great impetus and challenges for the integrated circuit (IC) industry.[1] Cutting-edge technology has reduced the effective size of field-effect transistors (FETs) down to sub-10 nm, or even sub-5 nm. Meanwhile, suppressing the short channel effect (SCE) and the resulting increase in off-state leakage current have become the main technical challenges of traditional planar transistors.[2] Innovative device structures have been developed to solve these problems, including FinFET,[3,4] gate-all-around FET (GAAFET),[5–7] multi-bridge channel FET (MBC-FET), and complementary FET (C-FET).[8–10] The enhanced gate controllability of the channel leads to reduced SCEs and current leakage. FinFET has been successfully applied to the sub-10 nm node while facing the technical challenges of a high height-to-width ratio due to scaling down.[11] The GAAFET-based MBC-FET structure has become a promising candidate for the next-generation sub-5 nm node, and C-FET will become a powerful alternative to the sub-2 nm node. However, existing Si-based MBC- and C-FETs face challenges such as non-uniform nanosheet geometry and drive current trade-offs.[8] The complex processing of integrating p- and n-type FETs also make a monolithic integration extremely difficulton a single Si substrate.[9,10]

With a given gate length, utilizing certain semiconductor characteristics, including heavier effective mass, larger bandgap, uniform atomic thickness, and lower in-plane dielectric constant, can minimize the magnitude of direct source-to-drain tunneling current, which is desired to solve SCE .[2] As a result, layered 2D semiconductors such as semiconductive transition metal dichalcogenides (TMDs) have become promising alternatives to Si and have been extensively explored.[12–22] The inherent layered structure of TMDs allows precise control of the thickness at the atomic level, which is a highly desired feature for the electrostatic control of ultra-short transistors.[23,24] For example, compared to Si in the sub-5 nm scaling node, MoS_2 displays much lower source-drain current leakage due to its larger electron effective mass, lower in-plane dielectric constant,

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and shorter electrostatic characteristic length.[25–29] Such device physical properties and characteristics make MoS_2 transistors a potential candidate for solving the ultimate gate-length scaling limitation. Zhou et al. reported a two-level-stacked MBC-FET based on MoS_2 channel material with low sub-threshold swing, extremely small leakage current and relatively high drive current, demonstrating the great potential of the MoS_2 MBC-FET.[30] Hu et al. demonstrated an experimental C-FET with a voltage gain of 10 V/V at V_{DD} = 3 V, which was constructed using n-type MoS_2 and p-type WSe_2 as the channel materials.[31] However, these devices were fabricated using the mechanically exfoliated flakes stacked by a transfer method, which lacks practicality for industrial applications.

To eliminate the issues mentioned above, we fabricated MBC-FET and C-FET based on wafer-scale chemical vapor deposition (CVD) grown 2D semiconductors. These devices were prepared by sophisticated transfer techniques and improved fabrication processes. Compared with conventional MoS_2 FETs, the carrier mobility of MoS_2 MBC-FET is 2.3 times higher, and the sub-threshold swing is 70% smaller, which has overcome the disadvantage of low drive current in TMD-based FETs. C-FET was fabricated by 3D integrating n-type MoS_2 and p-type $MoTe_2$ films, exhibiting a voltage gain of 7 V/V when V_{DD} = 4 V. Moreover, the technologies of layer-stacking and device processing with high repeatability and maturity can be easily repeated vertically for 2D semiconductors, and also advantageous for future scaling down of our demonstrated MBC-FETs and C-FETs.

2. Results and Discussion

In this work, wafer-scale n-type MoS_2 and p-type $MoTe_2$ were chosen as the channel materials, and both were synthesized by CVD methods. Detailed material information including optical microscopic images, Raman spectra and atomic force microscopy (AFM) characterizations are shown in Figures S1–S4, Supporting Information. The 3D schematic structure (**Figure 1**a) exhibits that MBC-FET consists of two parallel MoS_2 channels wrapped by the gate. The fabrication process of our MoS_2 MBC-FET is described in Figure S5, Supporting Information. Figures 1b and 1c show the device's optical microscopic images and cross-sectional schematic diagram, respectively, and Figure 1d displays a high-resolution transmission electron microscopy (HRTEM) image of the cross-sectional stacked structure of the MBC-FET. The corresponding energy-dispersive X-ray spectroscopy (EDS) images are shown in Figure S6, Supporting Information. The HRTEM image clearly shows the distribution of the MoS_2 channel, gate metal, and gate dielectric.

Before the electrical investigation of MBC-FET, a comparison between the single-gate and the dual-gate modes was made (Figure S7, Supporting Information) to clarify that the dual-gate mode possesses a better electrostatic control, which has also been demonstrated in previous works.[27,28] We then investigated the thickness-dependent (1–4 layers) performance of MoS_2 FETs under the dual-gate mode. The experimental results shown in Figure S8, Supporting Information, indicate that tri-layer (3L) MoS_2 dual-gate FETs possess a balanced electrical performance. Therefore, 3L-MoS_2 was chosen as the channel material for further investigation of MBC-FETs.

In order to measure the electrical properties of single-gate, dual-gate, and MBC-FET in one device for a fair comparison, we separated the source and drain electrodes of the two MoS_2 channels into individual ones (Figure S9, Supporting Information), which enable more convenient electrical connections. **Figures 2**a–f represent the transfer and output characteristics of the single-gate, dual-gate, and MBC-FET, respectively. When V_{DS} = 1 V and V_G = 2 V, the drive current I_D of the single-gate mode and dual-gate mode were only 0.6 µA and 3.2 µA, respectively, but the drive current of the MBC-FET booted up to 45 µA, as shown in Figure 2a–c. The OFF-state current of the MBC-FET was only 10^{-13} A; thus, a high ON/OFF ratio was also achieved in MBC-FET. Moreover, the saturation current of MBC-FET was 112 µA at V_G = 2 V, which is much higher than that of single-gate FET (1.3 µA) or dual-gate FET (3.1 µA). More detailed statistical data for single-gate, dual-gate, and MBCFETs were summarized in Figures S10 and S11, Supporting Information. The ON-state current (I_{ON}), threshold voltage (V_{TH}), sub-threshold swing (SS), mobility (μ) and ON/OFF ratio were all extracted and shown in Figure 2g. Compared with the single-gate and dual-gate MoS_2 FETs, the overall performance of MBC-FET was significantly improved, reflected by an I_{ON} of about 60 µA at V_{DS} = 1 V and V_G = 2 V, and a large ON/OFF ratio (10^9). The V_{TH} of MBC-FETs is located in an ideal range which is preferable for logic circuit applications. It is also noticed that the average mobility of MBC-FETs increases slightly, which can be ascribed to the quantum confinement effect in the dual-gate or MBC-FET structure, which can suppress interface trap density and carrier scattering at dielectric-MoS_2 interfaces.[32]

While the MBC-FET was realized by connecting the individual electrodes of two parallel MoS_2 channels together, one could also connect these electrodes in different ways to obtain various types of logic circuits. **Figure 3**a,b shows the optical microscopic image and circuit structure of a vertical inverter, which was realized by connecting the source and gate electrodes of the top transistor together to form the load transistor and connecting the source electrode of the top transistor with the drain electrode of the bottom transistor. The middle gate was grounded to screen the influence of top and bottom gate electrodes on the transistors on the other side. Figure 3c shows the voltage switching performance of such a vertical inverter. As V_{DD} increases from 1 to 3 V, the voltage gain increases from 1.8 to 6.8. The voltage gain was relatively low but can be improved by further optimization such as adjusting the V_{TH} or channel width/length ratio of the two MoS_2 FETs. Figure S12a, Supporting Information, shows that the noise margins (V_{DD} = 3 V) for low and high input voltages were NM_L = 0.25 V_{DD} and NM_H = 0.43 V_{DD}, respectively. The dynamic response of the vertical inverter at a frequency of 1 Hz is shown in Figure S12b, Supporting Information. The response time is beyond the measurement resolution, indicating that the device could work at a high frequency, considering the device size is tens of micrometers. Besides inverter, NAND and NOR logic circuits can also be formed following the same principle, as shown in Figure 3d–g. Due to the vertical stacking, the circuit area can be reduced by one-third compared with the traditional planar NAND and NOR circuits. These results suggest the substantial potential of our vertical stacked devices for building complex circuit systems.

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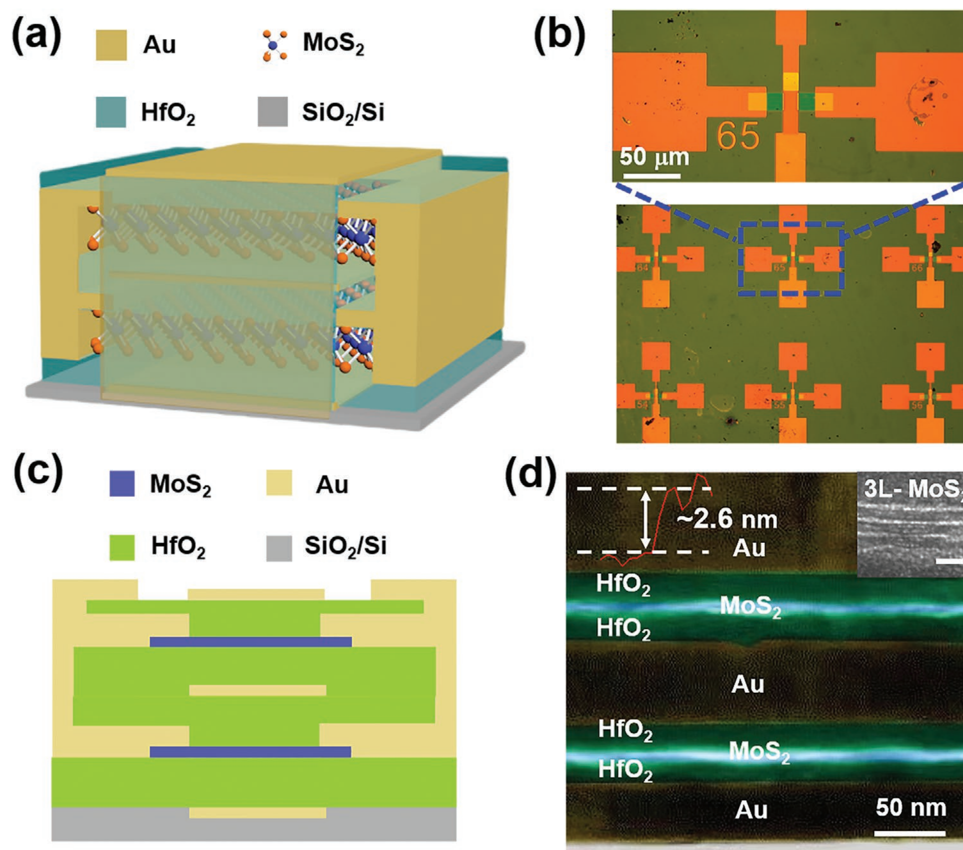

Figure 1. a) Schematic structure of a MoS_2 MBC-FET. The source/drain and gate electrodes of the two separated channels are connected. b,c) Optical images and cross-sectional schematic of MBC-FET. d) A cross-sectional HRTEM image of a typical MoS_2 MBC-FET, showing the distribution of MoS_2 channels, gate metals, and gate dielectric. The upper left inset is an AFM image of transferred tri-layer MoS_2 with a thickness of about 2.6 nm. The upper right inset is the HRTEM image of a tri-layer MoS_2, and the scale bar is 2 nm.

Furthermore, we demonstrate a C-FET by integrating n-type MoS_2 and p-type $MoTe_2$, whose 3D schematic structure was shown in **Figure** 4a. Its fabrication process flow is illustrated in Figure S13, Supporting Information. Figure 4b,c shows the optical images of C-FET. The n-type MoS_2 FET is located on the top layer which acts as a pull-down transistor, while the p-type $MoTe_2$ FET is located on the bottom layer acting as the pull-up transistor. The source of the MoS_2 FET is connected to the

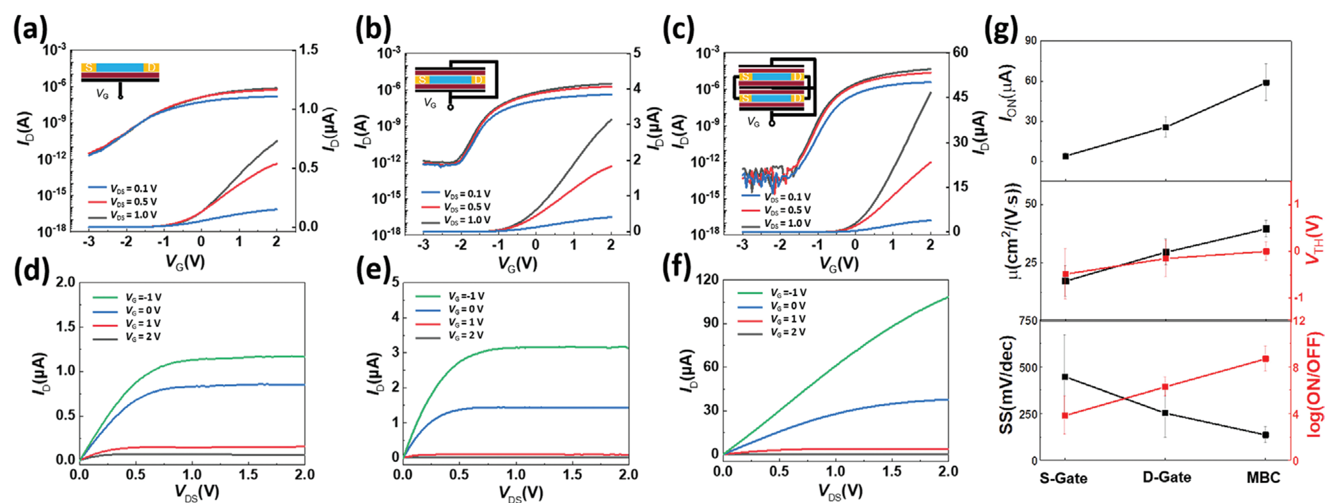

Figure 2. The transfer and output characteristics of single-gate MoS_2 FET (a,d), dual-gate MoS_2 FET (b,e), and MBC-FET (c,f), respectively. The insets are schematic illustrations of various electrical connections. g) A comparison of the electrical performance for single-gate FETs, dual-gate FETs, and MBC-FETs based on MoS_2 device arrays.

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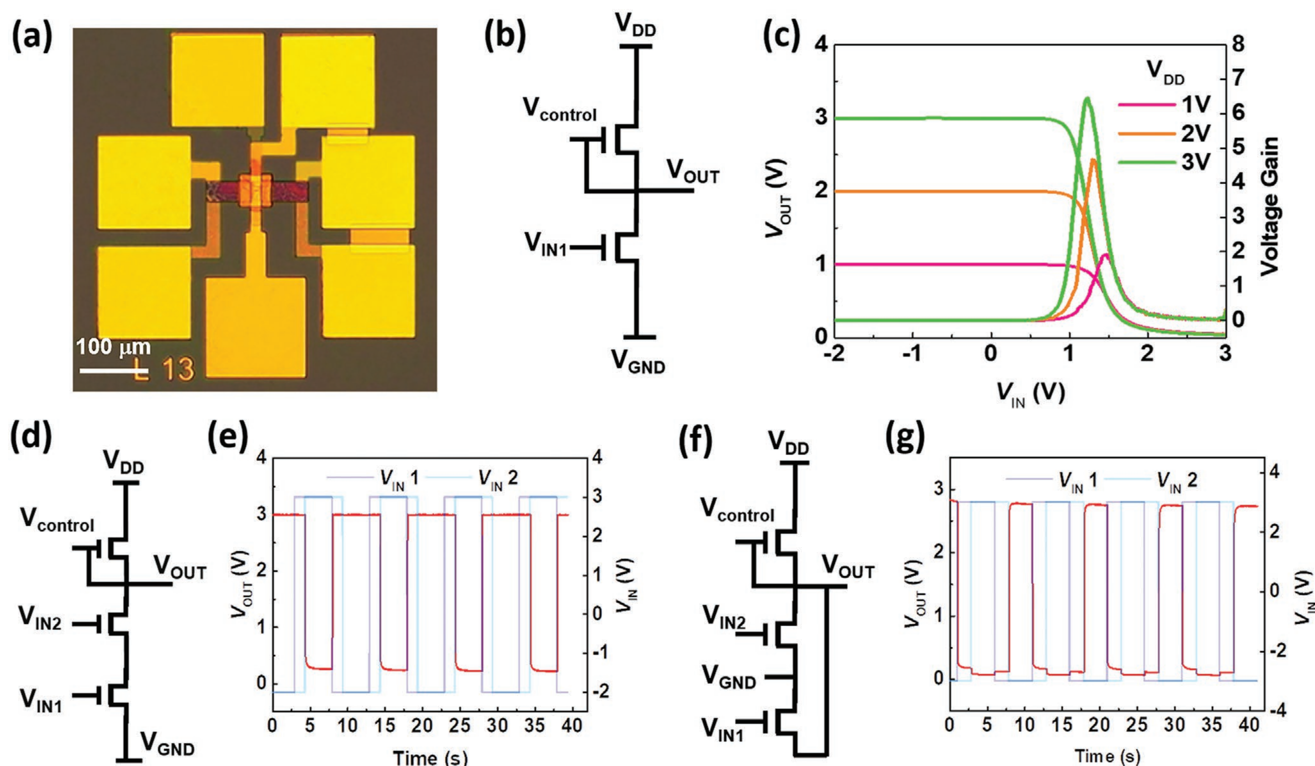

Figure 3. a,b) Optical image and circuit structure of vertical inverter based on n-type MoS_2 FETs. c) Voltage transfer characteristics and voltage gain of vertical inverter with a bias from 1 to 3 V. d,f) Circuit structure of NAND and NOR logic circuits, respectively. e,g) Dynamic response of NAND and NOR logic circuits at a frequency of 1 Hz, respectively, showing the unambiguous NAND and NOR functionalities.

drain of the $MoTe_2$ FET through via-holes, acting as an output. The middle gate is the input of the C-FET, which controls the channels of both top and bottom transistors. The cross-sectional schematic diagram of the C-FET is shown in Figure 4d. To verify the structure of the C-FET, we used a focused ion beam (FIB) to cut the 65 nm thick sample through the channel and the V_{DD} area and performed TEM measurements. Figures 4e and 4f present the cross-sectional HRTEM images obtained from the channel area and V_{DD} area, respectively, which show distinct layered structures. Obviously, the thickness of MoS_2 was about 3 nm, and the thickness of $MoTe_2$ was about 9 nm. The detailed EDS image corresponding to Figure 4e is given in Figure S14, Supporting information, showing the spatial distribution of C-FET chemical elements.

The transfer and output characteristics of the p-type $MoTe_2$ FET are shown in **Figures 5**a and 5b, respectively. When V_{TG} was swept from −5 to 5 V, $|I_{DS}|$ decreased from 1.43 μA to 4.3 nA under 1 V drain bias. The current ON/OFF ratio of the p-type $MoTe_2$ FET was about 325. The mobility and sub-threshold swing extracted from the transfer curves were 0.34 $cm^2\ V^{-1}\ s^{-1}$ and 103 mV dec^{-1}, respectively. Due to the pinch-off effect in the $MoTe_2$ FET with a channel length of 20 μm, the output curves were sub-linear at small V_{DS} and saturated at large V_{DS}. Figure 5c,d displays the transfer and output characteristics of the n-type MoS_2 FET. The transfer curve shows that a large current ON/OFF current ratio around 10^6 can be achieved at V_{DS} = 1 V, and the sub-threshold swing is about 370 mV dec^{-1}. The p-type $MoTe_2$ FET and the n-type MoS_2 FET were then connected to form a complementary inverter. Figure 5e shows the voltage transfer characteristics and voltage gain of the C-FET as a function of the input voltage, with a bias voltage varying from 1 V to 4 V. The p-type $MoTe_2$ FET and n-type MoS_2 FET were controlled by the same gate that served as the input voltage electrode (V_{IN}). When V_{IN} was low, the $MoTe_2$ FET was turned ON and the MoS_2 FET was OFF, and the output voltage was at a high level. When V_{IN} was increased, $MoTe_2$ FET was turned OFF and MoS_2 FET was ON. The output voltage then transitioned to a low-level voltage. The voltage gain from 1 V to 4 V was extracted from the voltage transfer characteristics, showing that the peak voltage gain was 7 at V_{DD} = 4 V, similar to a previous report about TMD based C-FET.[31] At V_{DD} = 4 V, the noise margins for low and high input voltages were $NM_L = 0.1\ V_{DD}$ and $NM_H = 0.36\ V_{DD}$, respectively (Figure S16, Supporting Information). A mapping measurement (voltage gain at V_{DD} = 1 V) of a 5 × 5 C-FET array was also summarized in Figure S15, Supporting Information. The relatively low yield of our C-FETs was mainly ascribed to the peeling off of $MoTe_2$ during the lift-off processing, which can be further optimized by including an appropriate annealing process.

Moreover, the device was illuminated with wavelength of 500, 600, and 700 nm under a power density of 1.55 mW cm^{-2}, as shown in Figure 5f. Under the illumination, the shift of switch voltage V_M can be mainly ascribed to the photogating effect in the top MoS_2 channel. The shift was more pronounced with a shorter wavelength, mainly because of stronger light absorption in monolayer MoS_2 which has a 1.8 eV direct bandgap.[33–36] The photogating induced photocurrent then provided a stronger driving capability to the pulldown MoS_2 transistor (nFET) to

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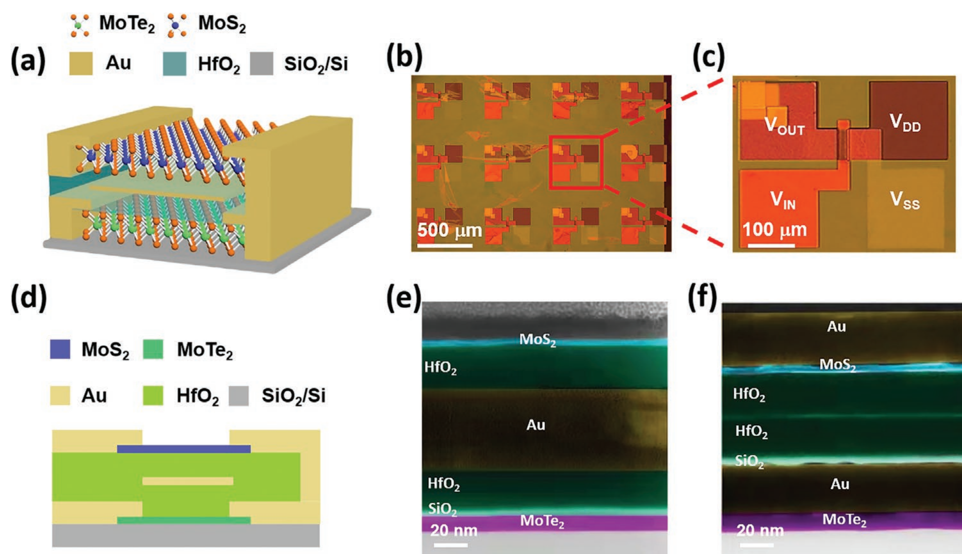

Figure 4. a) Schematic structure of C-FET. The top n-type MoS_2 FET and bottom p-type $MoTe_2$ FET are controlled by the middle Au gate. b,c) Optical images of C-FET. d) Schematic structure of cross-sectional view of C-FET. e,f) Cross-sectional high-resolution TEM images of channel area and V_{DD} area of the same C-FET.

shift V_M. The results indicated that our vertical stacked C-FET device based on 2D semiconductors can also convert the light signal to a digital signal at one step, demonstrating a potential optical sensing-processing application in the future.

3. Conclusion

Large-scale MBC-FET and C-FET based on n-type MoS_2 and p-type $MoTe_2$ were demonstrated. Compared with single-gate FET and dual-gate FET with one MoS_2 channel, the electrical performance of MBC-FET with two MoS_2 channels was greatly improved, including drive current, carrier mobility, subthreshold swing and ON/OFF ratio. Meanwhile, based on the vertically stacked parallel MoS_2 channels, we fabricated NAND and NOR logic circuits with a smaller footprint. Furthermore, the voltage gain of C-FET realized by 3D integrated n-type MoS_2 FET and p-type $MoTe_2$ FET was about 7 V/V when V_{DD} = 4 V. The V_M voltage could be adjusted by light illumination under different wavelengths. The exploration of large-scale MBC-FET

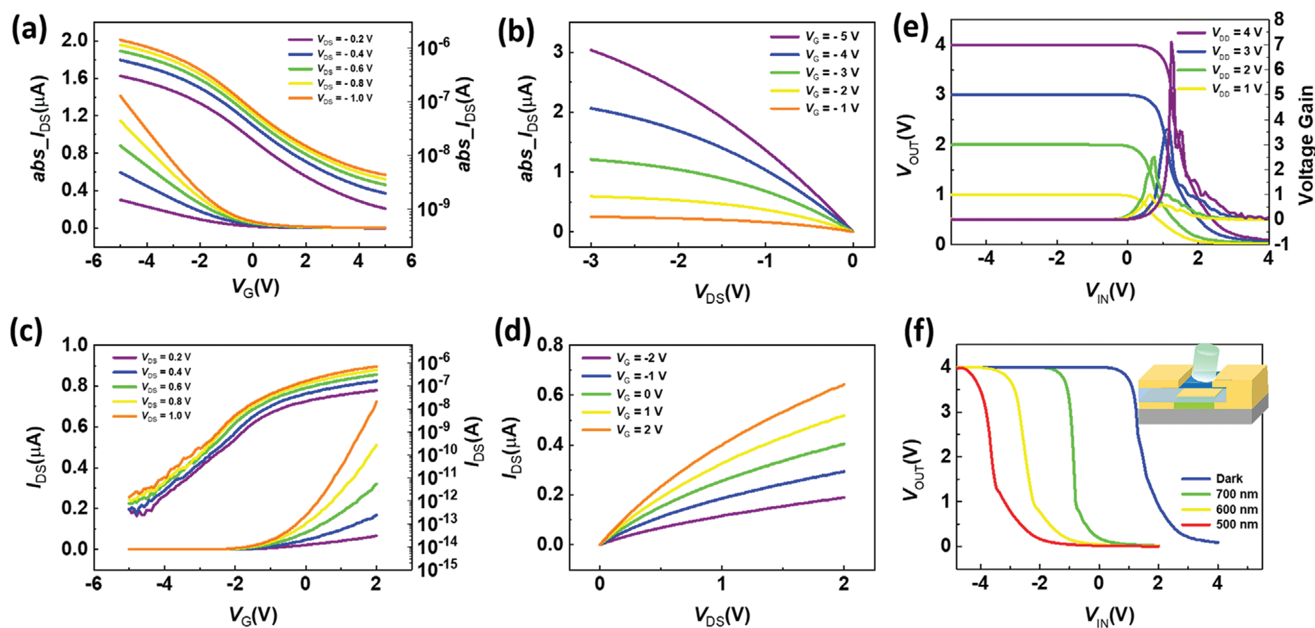

Figure 5. Transfer and output characteristics of the p-type $MoTe_2$ FET (a,b) and n-type MoS_2 FET (c,d), respectively. e) Voltage transfer characteristics and voltage gain of C-FET with a bias from 1 to 4 V. f) Voltage transfer characteristics of C-FET under illumination with wavelengths of 500, 600, and 700 nm under a power of 289.5 μW.

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and C-FET using 2D semiconductors will pave the way for more application opportunities in next-generation devices and circuits.

4. Experimental Section

Synthesis of Wafer-Scale MoS_2: The growth of monolayer MoS_2 was carried out in the two-temperature-zone CVD system. MoO_3 (Alfa Aesar 99.95%) and sulfur (Alfa Aesar 99.95%) powder were used as the precursors. The sulfur powder was placed in zone 1 and the MoO_3 in zone 2. The distance between zone 1 and zone 2 was 30 cm. Sapphire substrate was placed face-down above the MoO_3 source, and 300 sccm Ar gas was used as the carrier gas. The MoO_3 powder, S powder and substrate were heated to 180, 650 and 650 °C, respectively.

Synthesis of Wafer-Scale 2H-$MoTe_2$: First, 4 nm Mo was deposited on the SiO_2/Si by magnetron sputtering. Then, the deposited Mo was tellurized at 650 °C for 2 h in a CVD furnace, and 4 sccm Ar gas and 5 sccm H_2 gas were used as the carrier gases.

Transfer Process of Wafer-Scale MoS_2: First, a double layer MMA/PMMA (Aladdin, 99%) was spin-coated on monolayer MoS_2 and baked at 180 °C. Thermal release tape (TRT) was pressed firmly on the PMMA/MMA/MoS_2. The TRT/PMMA/MMA/MoS_2 stack was then mechanically peeled from the substrate through deionized water. Afterward, the whole stacked film was pressed onto the target substrate in the vacuum stacking setup and then heated at 130 °C for 30 min. The TRT was released from the substrate, and the PMMA/MMA was removed by acetone. The transfer of multi-layer MoS_2 was achieved by repeating the above process. Finally, annealing at 200 °C for 2 h was applied in a vacuum chamber to improve the adhesion between MoS_2 and the substrate.

Fabrication Process of MBC-FET and C-FET: Their detailed fabrication process flows can be found in Figures S5 and S13, Supporting Information, respectively.

Characterization and Electrical Measurement: Raman spectra were performed under a 532 nm laser at a spot size of 1 µm. AFM imaging was performed in atmosphere under tapping mode. HRTEM imaging and EDS characterization were carried out using an FEI Talos F200x instrument with an acceleration voltage of 200 kV. The electrical measurement was performed with an Agilent B1500A semiconductor analyzer.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

2D semiconductors, complementary field-effect transistors, MoS_2, $MoTe_2$, multi-bridge channel field-effect transistors

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